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EXAMINER	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/541,187	YAMASAKI, NOBUYUKI	
	Examiner	Art Unit	
	TAMMY LEE	2195	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 August 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-3 and 5-15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3 and 5-15* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 June 2005* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *6/30/05, 6/5/08, 6/18/08, 1/27/10*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application.
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-3, 5-15 are pending for examination.

Drawings

2. Figure 8 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claims 1-3, 5-15 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

a. The claim language in the following claims is not clearly understood:

i. As per claim 1, recites the limitation "the current context" in lines 22-23. There is insufficient antecedent basis for this limitation in the claim.

Line 36, it is unclear which context they are referring to "restoring a context from the context cache" and "saving a context from the register file" (i.e. are they the new context and the current context?)

ii. As per claim 2, it is unclear if "the context switch bus has a bus" refers to only a restore bus or a save bus (i.e. can a bus be any other context switch buses?)

iii. As per claims 10, 14, 15 have the same deficiency as claim 1 above.

Claim Rejections - 35 USC § 101

35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

4. Claims 14-15 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter.

5. Claim 14 cites "a context switching program", which implies that Applicant is claiming a system of software, per se, lacking the hardware necessary to realize any of the underlying functionality. Therefore, claim 14 is directed to non-statutory subject matter as computer programs, per se, i.e. the descriptions or expressions of the programs, are not physical "thing." They are neither computer components nor statutory processes, as they are not "acts" being performed.

6. Claim 15 cites "compute-readable recording medium". The specification is silent regarding the meaning of this term. Thus, applying the broadest reasonable interpretation in light of the specification and taking into account the meaning of the words in their ordinary usage as they would be understood by one of ordinary skill in the art (MPEP 2111), the claim as a whole cover both transitory and non-transitory media. A transitory medium does not fall into any of the 4 categories of invention (process, machine, manufacture, or composition of matter).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 1, 3, 5-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Joy et al US Patent 6,351,808 (hereafter Joy) in view of Cui et al (IDS "Parallel replacement mechanism for multithread", 1997 pages 338-343) (hereafter Cui).

8. As per claim 1, Joy teaches the invention substantially as claimed including a context switching unit for switching a plurality of contexts, the context switching unit comprising (col 6, lines 33-49, FIG. 12, col 25, lines 50-67):

a register file having stored a context related to a thread to be executed by an arithmetic logic unit or a memory access unit, the register file comprising a read port, a

write port, a context-switching read port, and a context-switching write port (FIG. 12, register file 1248, 1250, ALU 1234, 1236, memory access unit 1222, col 25, lines 50-67, col 26, lines 1-46, read/write port connected to each unit);

a context cache for caching a context, the context cache comprising a read port and a write port, being connected directly to the register file, and being contained in a central processing unit in a on-chip manner (FIG. 8, 810, cache which stores contexts for thread 0 and 1, FIG. 12, 1256, which is directly connected to register file 1248);

a context switching bus for connecting the register file and the context cache, the context switching bus comprising a restore bus and a save bus for connecting the read port and the write port of the context cache to the context-switching write port and the context-switching read port of the register file respectively (FIG. 12, bus connecting the register file (1248) and the context cache (1256));

and a thread control unit for controlling data transfer between the context cache and the register file, the thread control unit comprising a thread identifier table for storing a thread identifier for identifying the context of a thread stored in the context cache and being connected in parallel with the arithmetic logic unit and the memory access unit (FIG. 8, col 17, lines 30-67, Thread ID, identifying context of a thread stored in cache, FIG. 12 ALU and memory access unit);

the identifier of a new thread to be interchanged (col 15, lines 49-67);

the thread control unit obtains a restore address where a new context to be interchanged is stored in the context cache and the save register identifier indicating the location where the current context is stored in the register file, by searching through the

thread identifier table in accordance with the thread identifier (col 15, lines 49-67, col 27, lines 11-36, individual plane for register file 1300 represent a separate context);

the thread control unit sends the obtained address to the context cache (col 15, lines 49-67, FIG. 8);

the context cache, in accordance with the address given by the thread control unit (FIG. 8, 810, cache which stores contexts for thread 0 and 1, FIG. 12, 1256, which is directly connected to register file 1248).

Joy does not explicilty teach wherein the thread control unit receives a context switch instruction for executing a save operation and a restore operation concurrently and when a context switch which executes both a context save operation and a context restore operation in parallel occurs; sends the register identifier to the register file concurrently; the register file, in accordance with the register identifier given by the thread control unit, outputs the data of the context to be saved from the context-switching read port and, concurrently writes the data of the context to be restored, sent from the read port of the context to the context-switching write port through the restore bus, in the register corresponding to the register identifier; concurrently writes the data of the context to be saved sent from the context-switching read port of the register file to the write port via the save bus; and the context switching unit switches contexts by executing an operation for restoring a context from the context to the register file and an operation for saving a context from the register file to the context concurrently.

However, Cui teaches wherein the thread control unit receives a context switch instruction for executing a save operation and a restore operation concurrently and

when a context switch which executes both a context save operation and a context restore operation in parallel occurs (pg. 340, 3. overlapped replacement mechanism, FIG. 3_1, a control unit concurrently executing saving and restoring of contexts through the restore/save bus);

sends the register identifier to the register file concurrently (pg. 340, FIG. 3_1, load/save context can be done concurrently during context switching, temp1 and temp2 are two register sets to preserve unload/load threads);

the register file, in accordance with the register identifier given by the thread control unit, outputs the data of the context to be saved from the context-switching read port and, concurrently writes the data of the context to be restored, sent from the read port of the context to the context-switching write port through the restore bus, in the register corresponding to the register identifier (pg. 340, FIG. 3_1, load/save context can be done concurrently during context switching, temp1 and temp2 are two register sets to preserve unload/load threads);

outputs the data of the context to be restored from the read port (pg. 340, lines 10-30);

concurrently writes the data of the context to be saved sent from the context-switching read port of the register file to the write port via the save bus (pg. 340, FIG. 3_1, load/save context can be done concurrently during context switching);

and the context switching unit switches contexts by executing an operation for restoring a context from the context to the register file and an operation for saving a

context from the register file to the context concurrently (pg. 340, FIG. 3_1, load/save context can be done concurrently during context switching).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate Cui's teaching to Joy's invention in order to reduce thread replacement overhead by restoring and saving concurrently (pg. 340, lines 15-30).

9. As per claim 3, Joy and Cui teach The context switching unit according to claim 1, and Joy teaches wherein the thread control unit comprises as many thread identifier tables as required to identify contexts cached in the context cache (FIG. 8, col 17, lines 30-67, Thread ID identify contexts cached in the context cache).

10. As per claim 5, Joy and Cui teach The context switching unit according to claim 1, Joy teaches wherein the thread control unit saves the context of the current thread from the register file to the context cache (FIG. 8, col 17, lines 30-67, Thread ID);

to automatically interchange a required number of data items between the register file and the context cache, when software, such as an operating system, issues a swap instruction for interchanging contexts, including a thread identifier as an operand, if the swap instruction is executed (col 15, lines 49-67, col 18, lines 1-10).

Joy does not explicitly teach sends the context of a new thread from the context cache to the register file concurrently.

Cui teaches sends the context of a new thread from the context cache to the register file concurrently (pg. 340, FIG. 3_1, load/save context can be done concurrently during context switching, temp1 and temp2 are two register sets to preserve unload/load threads).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate Cui's teaching to Joy's invention in order to reduce thread replacement overhead by restoring and saving concurrently (pg. 340, lines 15-30).

11. As per claim 6, Joy and Cui teach The context switching unit according to claim 1, Joy does not explicitly teach wherein the thread control unit transfers the data of a context from the register file to the context cache and does not transfer the data of a context from the context cache to the register file, when software, such as an operating system, issues a backup instruction for saving a context, including a thread identifier as an operand, if the backup instruction is executed.

Cui teaches wherein the thread control unit transfers the data of a context from the register file to the context cache and does not transfer the data of a context from the context cache to the register file, when software, such as an operating system, issues a backup instruction for saving a context, including a thread identifier as an operand, if the backup instruction is executed (pg. 340, 3. overlapped replacement mechanism, FIG. 3_1, a control unit concurrently executing saving and restoring of contexts through the restore/save bus).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate Cui's teaching to Joy's invention in order to reduce thread replacement overhead by restoring and saving concurrently (pg. 340, lines 15-30).

12. As per claim 7, Joy and Cui teach The context switching unit according to claim 1, Joy does not explicitly wherein the thread control unit transfers the data of a context from the context cache to the register file and does not transfer the data of a context from the register file to the context cache, when software, such as an operating system, issues a restore instruction for restoring a context, including a thread identifier as an operand, if the restore instruction is executed.

Cui teaches the thread control unit transfers the data of a context from the context cache to the register file and does not transfer the data of a context from the register file to the context cache, when software, such as an operating system, issues a restore instruction for restoring a context, including a thread identifier as an operand, if the restore instruction is executed (pg. 340, 3. overlapped replacement mechanism, FIG. 3_1, a control unit concurrently executing saving and restoring of contexts through the restore/save bus).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate Cui's teaching to Joy's invention in order to reduce thread replacement overhead by restoring and saving concurrently (pg. 340, lines 15-30).

13. As per claim 8, Joy and Cui teach A central processing unit comprising: a context switching unit according to claim 1 (FIG. 12);

an instruction cache for caching an instruction and a data cache for caching data (FIG. 12, 1212);

an instruction fetch unit for fetching an instruction from the instruction cache and decoding the instruction (FIG. 12, 1216, 1214);

an arithmetic logic unit for performing an operation in accordance with an instruction stored in the register file and writing the result of the operation back in the register file (FIG. 12, 1234, 1236, 1248);

a memory access unit for receiving an operand and an instruction from the register file, accessing the data cache, and executing a load or store operation (FIG. 12, 1222, 1232);

and an arithmetic bus for connecting the register file, the arithmetic logic unit, the memory access unit, and the thread control unit in parallel (FIG. 12, buses between the units).

14. As per claim 9, Joy and Cui teach The central processing unit according to claim 8, Joy teaches wherein the memory access unit sends an address and data to the data cache and stores the data in the data cache when a store instruction is given, and the memory access unit sends an address to the data cache, reads data from the data cache (FIG. 8, col 17, lines 30-53, col 18, lines 1-35).

Joy does not explicitly teach and writes the read data back into the register file when a load instruction is given.

Cui teaches and writes the read data back into the register file when a load instruction is given (pg. 340, lines 15-30).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate Cui's teaching to Joy's invention in order to reduce thread replacement overhead by restoring and saving concurrently (pg. 340, lines 15-30).

15. As per claim 10, it is a method claim of claim 1, thus it is rejected for the same reason as claim 1 above.

16. As per claim 11, it is a method claim of claim 5, thus it is rejected for the same reason as claim 5 above.

17. As per claim 12, it is a method claim of claim 6, thus it is rejected for the same reason as claim 6 above.

18. As per claim 13, it is a method claim of claim 7, thus it is rejected for the same reason as claim 7 above.

19. As per claim 14, it is a program claim of claim 1, thus it is rejected for the same reason as claim 1 above.

20. As per claim 15, it is a computer readable recording medium claim of claim 1, thus it is rejected for the same reason as claim 1 above.

21. Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Joy in view of Cui as applied to claim 1, and further in view of Suzuoki et al. US Patent 6,526,491 (hereafter Suzuoki).

22. As per claim 2, Joy and Cui teach The context switching unit according to claim 1, but does not explicitly teach wherein the context switching bus has a bus width greater than the bit width of the register file.

However, Suzuoki teaches a bus width greater than the bit width of the register file (FIG. 4, col 8, lines 42-61).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate Suzuoki's teaching to Joy and Cui's invention in order to accommodate a larger data flow from registers during processing by providing a larger width of buses than the registers (col 8, lines 42-61).

Conclusion

23. Any inquiry concerning this communication or earlier communications from the examiner should be directed to TAMMY LEE whose telephone number is (571)270-7773. The examiner can normally be reached on Monday through Friday 9:00 AM to 6:00 PM; with every other Friday off.

24. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Meng Ai An can be reached on 571-272-3756. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

25. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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